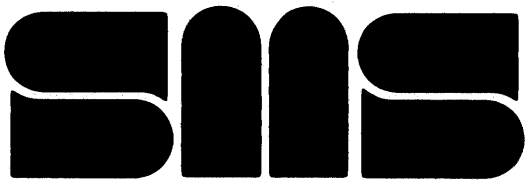


OMTI 5027C
2 of 7 VCO ENCODE DECODE CHIP
REFERENCE MANUAL
DECEMBER 1986

Scientific Micro Systems, Inc.

OMTI 5027C
2 of 7 VCO ENCODE
DECODE CHIP
REFERENCE MANUAL
DECEMBER 1986

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

LIST OF APPENDIX

OMTI 5027C 2 of 7 VCO ENCODE/DECODE

REFERENCE MANUAL

(PART #20527C)

REV.	REVISION HISTORY	PRINT DATE
	Original Issue	Dec 05, 1986

SECTION 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The OMTI 5027C 2 of 7 VCO/Encode/Decode chip provides all of the necessary functions needed to convert disk drives with 2 of 7 encoded serial data interfaces (i.e., ST412R and Integrated SCSI Drives) to NRZ data and clock. It contains an internal voltage controlled oscillator, phase-locked loop, encode/decode logic, Address mark generation and detection, and all the circuit required to perform a two level double amount write precompensation.

The OMTI 5027C is capable of operating at a data rate up to 10 megabits per second by proper selection of the external frequency and loop gain components. The need for a delay lines is eliminated for write precompensation by using a silicon delay element internal to this chip.

1.2 OMTI 5027C VCO/ENCODE/DECODE CHIP CAPABILITIES

* Data rate control to 10 megabits per second
* No internal loop gain or frequency determining function
* No external logic required
* Internal VCO and phase-locked loop
* 2 of 7 to NRZ and NRZ to 2 of 7 converters
* Internal address mark detection and generation logic
* Two level write precompensation circuitry
* Control for external filter/varactor diode
* 2 micron DLM CMOS Standard Cell Technology
* Power Down mode (portable market)
* 28-Pin PLCC Package

1.3 FUNCTIONAL OVERVIEW

Figure 1 illustrates the internal block diagram of the OMTI 5027C 2 of 7 VCO/Encode/Decode Chip. Each logic block is discussed in the following sections.

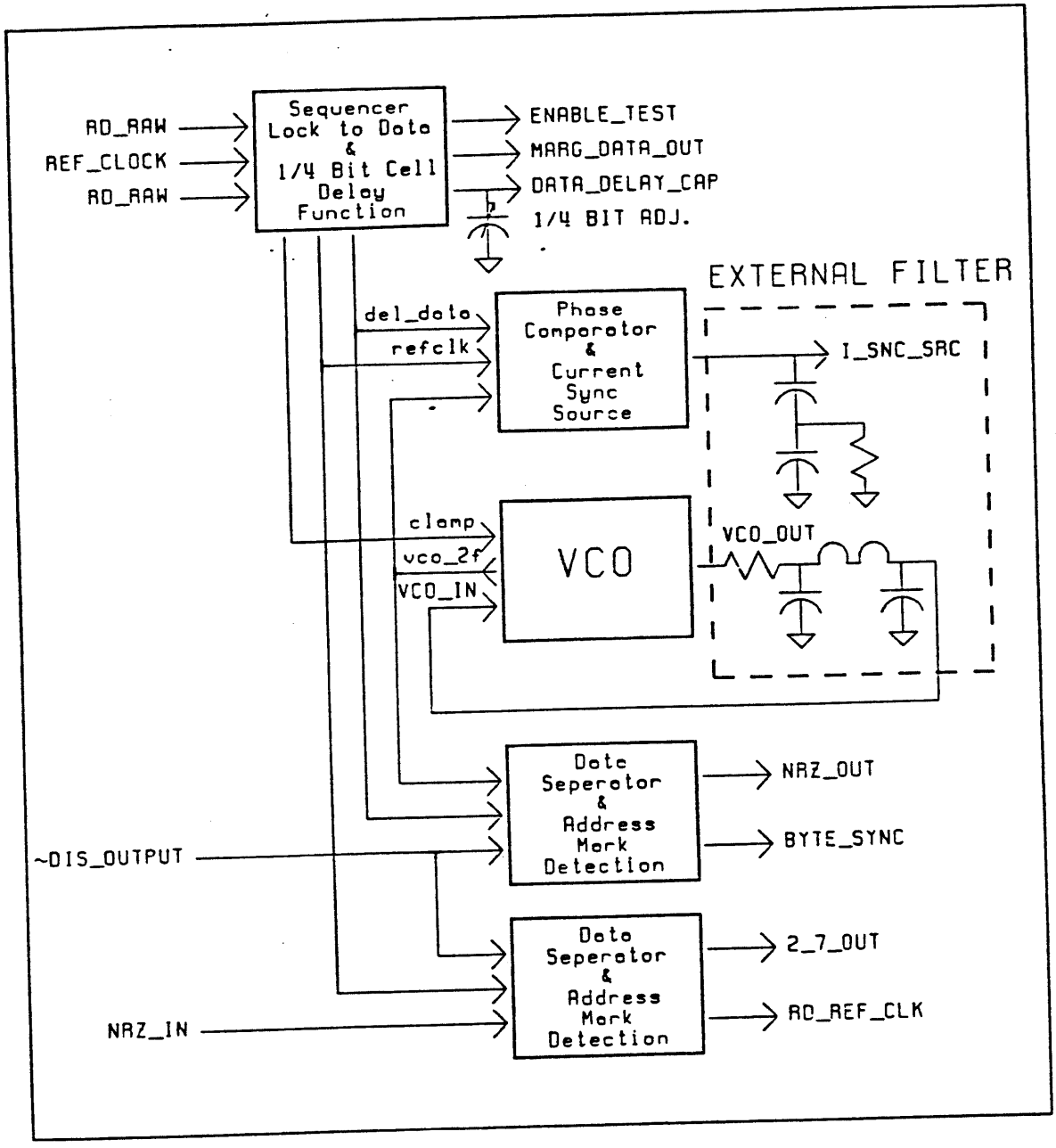


Figure 1. Internal Block Diagram

1.3.1 Sequencer, Lock to Data and 1/4-bit Delay

The sequencer is responsible for finding a VCO sync field and locking the VCO to the incoming RD_RAW data. A flow chart in figure 2 describes the states and there requirements for Lock-To-Data (LTD) and Search Address Mark (SAM). The 1/4-bit cell delay function is achieved by forcing a constant current into an external capacitor. When it reaches the threshold of a Schmidt trigger 1/4-bit delay should be reach. This function is used in the Phase Comparitor.

1.3.2 Phase Comparitor

The Phase Comparitor compares the phase of the REF_CLOCK with the VCO and creates a current in the I_SNC_SRC output pin proportional to the phase error. The I_SNC_SRC output pin should be connected to an external filter whose integrated voltage should control the frequency of the VCO varactor diode. At LTD time the Phase Comparitor switches from the REF_CLOCK to the RD_RAW input. At LTD time the VCO input is clamped and the VCO is disabled until two RD_RAW pulses have occurred at which time the clamp is released enabling the VCO to come up in phase with the RD_RAW incoming signal.

1.3.3 Filter VCO Control

The Filter VCO Control attenuates the high-frequency error components of the I_SNC_SRC phase error output and presents a control voltage to the VCO by controlling the varactor diode.

1.3.4 VCO

The Voltage Controlled Oscillator is a voltage to frequency converter used to provide a clock which is at the same frequency and phase as the REF_CLOCK or RD_RAW if LTD is asserted. The VCO frequency is determined by the I_SNC_SRC phase compare output passed thru the Filter VCO Control.

1.3.5 Data Separator and Address Mark Detect

The Data Separator generated a pulse from the delayed data and a clock generated by the VCO signal. This pulse is then converted from a 2 of 7 pattern to the NRZ_OUT signal. At SAM time a 2 of 7 pattern is searched for consisting of a nrz 62 with a pulse one clock delayed. This pattern is within the 2 of 7 encoding requirements but an illegal combination that will never be used in a normal data field. When this pattern is detected the Address Mark Found (AM_FOUND) signal is asserted and remains asserted until RD_GATE is de-asserted.

1.3.6 Write Encoder with Precompensation and Address Mark

This block converts the NRZ data (NRZ_IN) sampled by the rising edge of RD_REF_CLOCK into a 2 of 7 data stream (see encoding algorithm in table 1). When an address mark is to be written, AM_ENABLE is asserted during a NRZ_IN pattern of 62h. When this pattern is converted to 2 of 7, a clock pulse is shifted resulting in an illegal pattern which is used during read operations as a Address Mark. If the ~EN_PRECOMP input is asserted low, this chip will perform a two level precompensation based on the pattern which follows in table 2.

INPUT NRZ DATA	ENCODED DATA OUT
11	1000
011	001000
0011	00001000
10	0100
010	100100
0010	00100100
000	000100

Table 1. 2 of 7 Encode Algorithm.

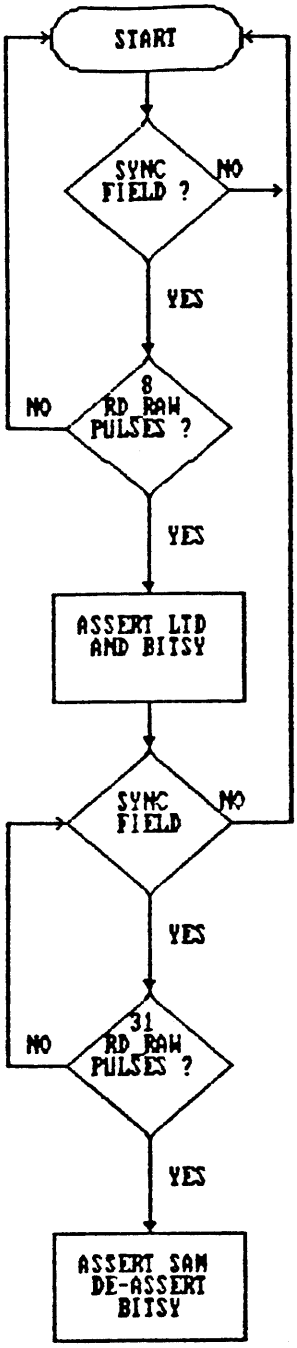
2 of 7 Encode Pattern										Precomp.	Precomp. Amount ~L_H_PRECOMP *	
previous			current		V	future				Type	0	1
0	0	1	0	0	1	0	0	0	1	Early	-2.5ns	-5ns
0	1	0	0	0	1	0	0	0	0	Early	-2.5ns	-5ns
0	1	0	0	0	1	0	0	1	0	Late	2.5ns	5ns
X	0	0	0	0	1	0	0	0	1	Late	2.5ns	5ns
0	0	1	0	0	1	0	0	0	X	Early Early	-5ns	-10ns
X	0	0	0	0	1	0	0	1	0	Late Late	5ns	10ns

* Amount of Precompensation is a function of silicon delay and therefore changes with process, temperature and voltage.

Table 2. Precompensation Table

APPENDIX A

READ CONTROL FLOW CHART



The Read Control Flow start by asserting RD_GATE. After RD_GATE is asserted the internal state machine will search for a sync field. To complete the sync field requirements, eight consecutive RD_RAW pulses of FFh data must be detected.

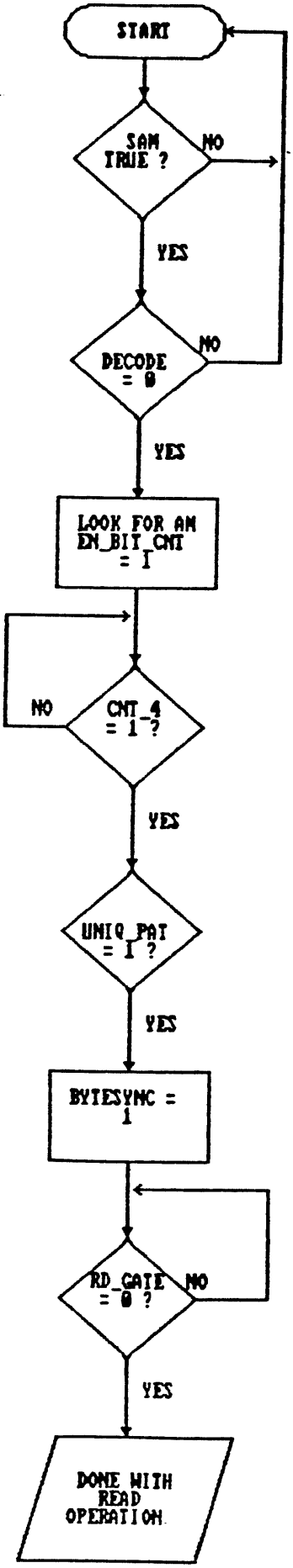
After the sync field requirements have been met, Lock-To-Data (LTD) and Bit-Sync (BITSY) will be asserted. The sequencer will remain looking for sync field data until a total of 31 RD-RAW pulses have been detected. While BITSY is asserted the internal RD_CLOCK can re-phase to align with the incoming RD_RAW data.

After a total of 31 RD_RAW pulses the sequencer will assert Search-Address-Mark (SAM) and de-assert BITSY. As SAM is asserted the Read-Reference-Clock (RD_REF_CLK) output will be synchronously switched from the write reference clock to the VCO reference clock which is synchronous with the NRZ_OUT data signal.

If at any time RD_GATE is de-asserted, the sequencer will return to the idle mode and wait for RD_GATE to be asserted again.

APPENDIX B

SAM STATE MACHINE FLOW CHART



When SAM is asserted, RD_RAW has been qualified as a sync field for 8 bytes. The SAM state machine determines if the previously found sync field is a valid preamble area. This decision is made by looking for a special, invalid 2 of 7 pattern which was written at format or at data field write update time. This unique pattern must exist at a specific location in order to qualify as a BYTE_SYNC pattern.

After the first decoded NRZ_OUT bit of a zero, the unique pattern flag must be asserted precisely four bit times later. If it is asserted, BYTE_SYNC will be asserted and the state machine will lock up and remain until RD_GATE is de-asserted. If the unique pattern was not set, the state machine will clear and wait for the next sync field to be qualified.

SECTION 3

INTERFACING

3.1 PIN DESCRIPTIONS

Symbol	Type	Pin #	Name and Function
NRZ_IN	I	1	NRZ Data In (Active High.) This serial data input carries data from the sequencer (OMTI 5050) and is encode to the 2 of 7 pattern during a write operation. This signal is sampled in the falling rising of RD_REF_CLK.
NRZ_OUT	O	2	NRZ Data Out (Active High.) This serial data tri-state output carries data from this chip to the sequencer (OMTI 5050) and is decode from the 2 of 7 pattern during a read operation. This signal is valid on the rising edge of RD_REF_CLK. This output is in tri-state mode when the ~DIS_OUTPUT is asserted low.
~L_H_COMP	I	3	Low High Precompensation (Active Low.) This internally pulled-up input is used to control the amount of precompensation when the ~EN_PRE_COMP input is asserted low. When this input is low, a lessor amount of precomp will be in effect. See table 2 for the amount of precomp in ns.
RD_REF_CLK	O	4	Read Reference Clock (Active High.) This tri-state output signal is multiplexed between WREFCLK, which is used to synchronize NRZ_IN on a write operation and RD_CLK, which is used to synchronize NRZ_OUT on a read operation. When transitioning between the two clocks (at SAM time) missing clocks will occurs but no glitches will appear. This output is in tri-state mode when the ~DIS_OUTPUT is asserted low.
RD_GATE	I	5	Read Gate (Active High.) This signal starts the read sequence by enabling the read control block to start searching for a sync field. This input may be asserted asynchroniously to data or any other input to this chip.

3.1 PIN DESCRIPTIONS

Symbol	Type	Pin #	Name and Function
WRT_GATE	I	6	Write Gate (Active High.) This input signal when asserted, enables the encoding of the NRZ_IN serial data input to be converted to the 2_7_OUT output pulse data signal.
REF_CLOCK	I	7	Reference Clock (Active High.) This input must have a free running clock at two times the NRZ data rate. This clock is used for encoding the 2 of 7 pattern from the NRZ_IN and also is used to lock the VCO at this frequency at any time SAM is not asserted.
AM_ENABLE	I	8	Address Mark Enable (Active High.) This input signal controls when an address mark is written on the disk during a format track or sector write update command. When this input is asserted with a NRZ_IN serial data pattern of 62h, a clock transition will be moved to create an illegal pattern.
BYTE_SYNC	O	9	Byte Synchronization (Active High.) This tri-state output is asserted after either the ID of DATA sync byte has been found. It determines the byte boundary for the NRZ_OUT serial data signal. The sync pattern must be the 62h with a clock transition shifted that followed the VCO sync field of FFh serial data. This output is in tri-state mode when the ~DIS_OUTPUT is asserted low.
MARG_DATA_OUT	O	10	Margin Data Output (Active High.) This output feeds data from the disk externally so it can be shifted in the window when doing a phase margin test.
MARG_DATA_IN	I	11	Margin Data Input (Active High.) This internally pulled-up input is the return path for the MARG_DATA_OUT signal after it has been delayed to determine margin analysis.

3.1 PIN DESCRIPTIONS

Symbol	Type	Pin #	Name and Function
~MARGIN_TEST	I	12	Margin Test (Active Low.) This internally pulled-up input when pulled low allows a margin test to be performed by multiplexing MARG_CLK_IN into VCO_2F and MARG_DATA-IN into DEL_DATA.
~EN_PRE_COMP	I	13	Enable Precompensation (Active Low.) This internally pulled-up input when asserted low enables a two level write precompensation of the 2_7_OUT pulses.
GROUND	I	14	Ground
~FORCE_LTD	I	15	Margin Test (Active Low.) This internally pulled-up input when pulled low allows a margin test to be performed by multiplexing MARG_CLK_IN into VCO_2F and MARG_DATA-IN into DEL_DATA.
RD_RAW	I	16	Read Raw Data (Active High.) This input is the raw digital 2 of 7 pulse information from the disk drive. This input is rising edge sensitive.
2_7_OUT	O	17	2 of 7 Output (Active High.) This tri-state output is the 2 of 7 pulses encoded from the NRZ_IN input while WRT_GATE is asserted. This output is in tri-state mode when the ~DIS_OUTPUT is asserted low.
DATA_DELAY_CAP	I	18	Data Delay Capacitor (Active Low.) This output when connected to an external capacitor determines the 1/4 bit cell delay required to separate data.
~DIS_OUTPUT	I	19	Disable output (Active Low.) This internally pulled-up input when pulled low tri-states all non-test outputs so multiple chips can be connected in parallel. This function also puts this chip in power down mode.

3.1 PIN DESCRIPTIONS

Symbol	Type	Pin #	Name and Function
MARG_CLK_OUT	O	20	Margin Clock Out (Active High.) This output signal is the locked VCO signal that can be delayed and fed back in the MARG_CLK_IN when performing a phase margin test.
MARG_CLK_IN	I	21	Margin Clock In (Active High.) This internally pulled-up input is the return path for the MARG_CLK_OUT after it has been delayed when performing a phase margin test.
TEST	O	22	Test This output is reserved for test functions.
VCO_IN	I	23	VCO Input (Active High.) This input signal is the feedback for the VCO from the VCO_OUT pin through an external LC network.
VCO_OUT	O	24	VCO Output (Active High.) This output is the driving signal for the VCO through an external LC network to the VCO_IN input.
I_SRC_SNK	O	25	Current Source Sink (Tri-State.) This output pin sources current when the phase comparitor indicates the VCO should speed up, and sinks current when the VCO frequency needs to slow down. The source/sink current is proportional to the I_ADJUST current pin.
ENABLE_TEST	O	26	Enable Test (Active High.) This output signal is used to calibrate the DATA_DELAY_CAP to achieve a 1/4 bit cell delay.
I_ADJUST	I	27	Current Adjust (Active High.) This input provides the current reference for the constant current control elements in the chip. This includes the I_SRC_SNK function and the 1/4 bit cell delay. An external resistor from V+ connected to this pin determines the current value.
V+	I	28	V +

3.2 PIN ASSIGNMENT

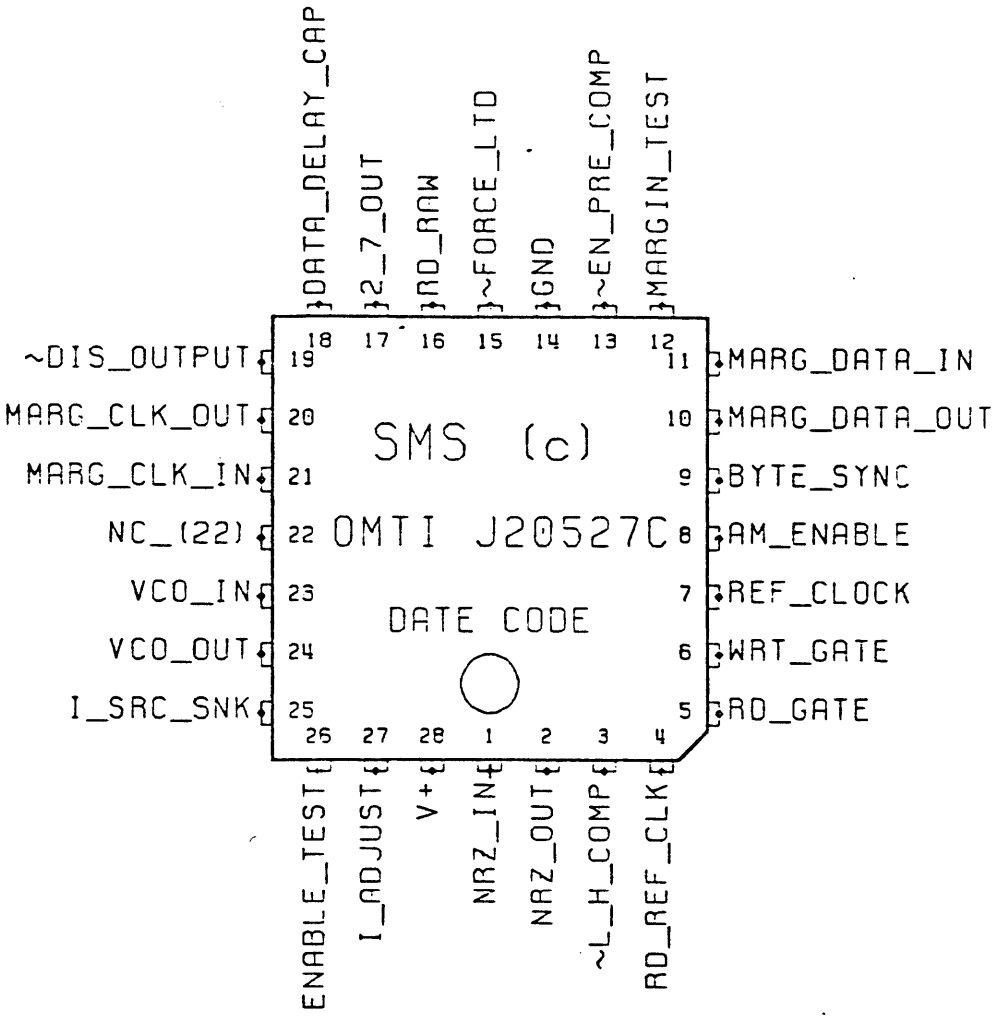


Figure 2. Pin Assignment

SECTION 4

D. C. CHARACTERISTICS

4.1 Absolute Maximum Ratings:

* Voltages on all pins with respect to GND range from -0.3 V to +7.0 V.

* Ambient operating temperature is 0 degrees C. to +70 degrees C.

* Storage temperature ranges from -65 degrees C. to +150 degrees C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

4.2 Standard Test Conditions:

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

* +4.75 V < VCC < +5.25 V

* GND = 0 V

* 0 degrees C. < TA < +70 degrees C.

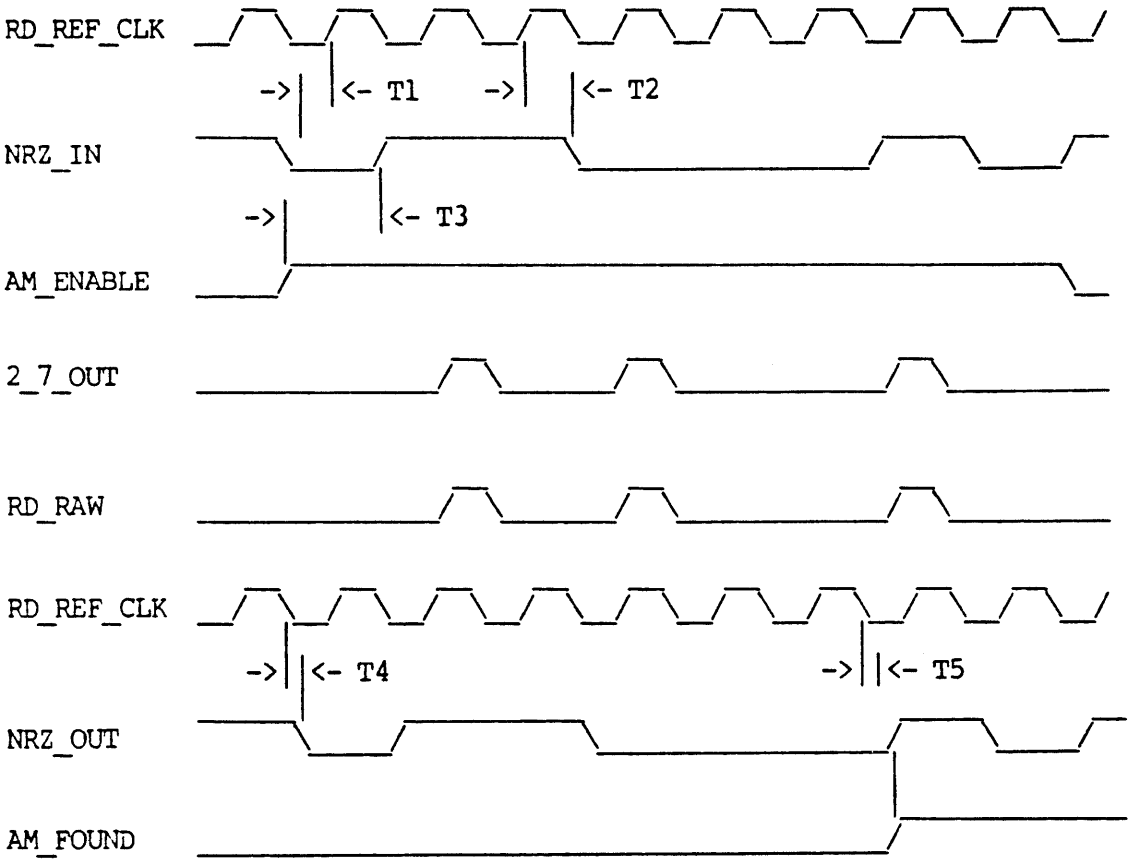
4.3 D.C. Characteristics:

Parameter	Min	Max	Unit	Condition	Notes
Input High Voltage	2	VCC	V		
Input Low Voltage	-0.3	0.8	V		
Output High Voltage	2.4	VCC	V		
Output Low Voltage		0.4	V		
Output Low Current	4.0		mA		
Output High Current	-4.0		mA		
Output Low Current	12.0		mA	I_SNC_SRC	
Output High Current	-12.0		mA	I_SNC_SRC	
Input Leakage	-30	10	uA		
Output Leakage		10	uA		
VCC Supply Current		50	mA		

SECTION 5

A. C. CHARACTERISTICS

5.1 Interface Timing



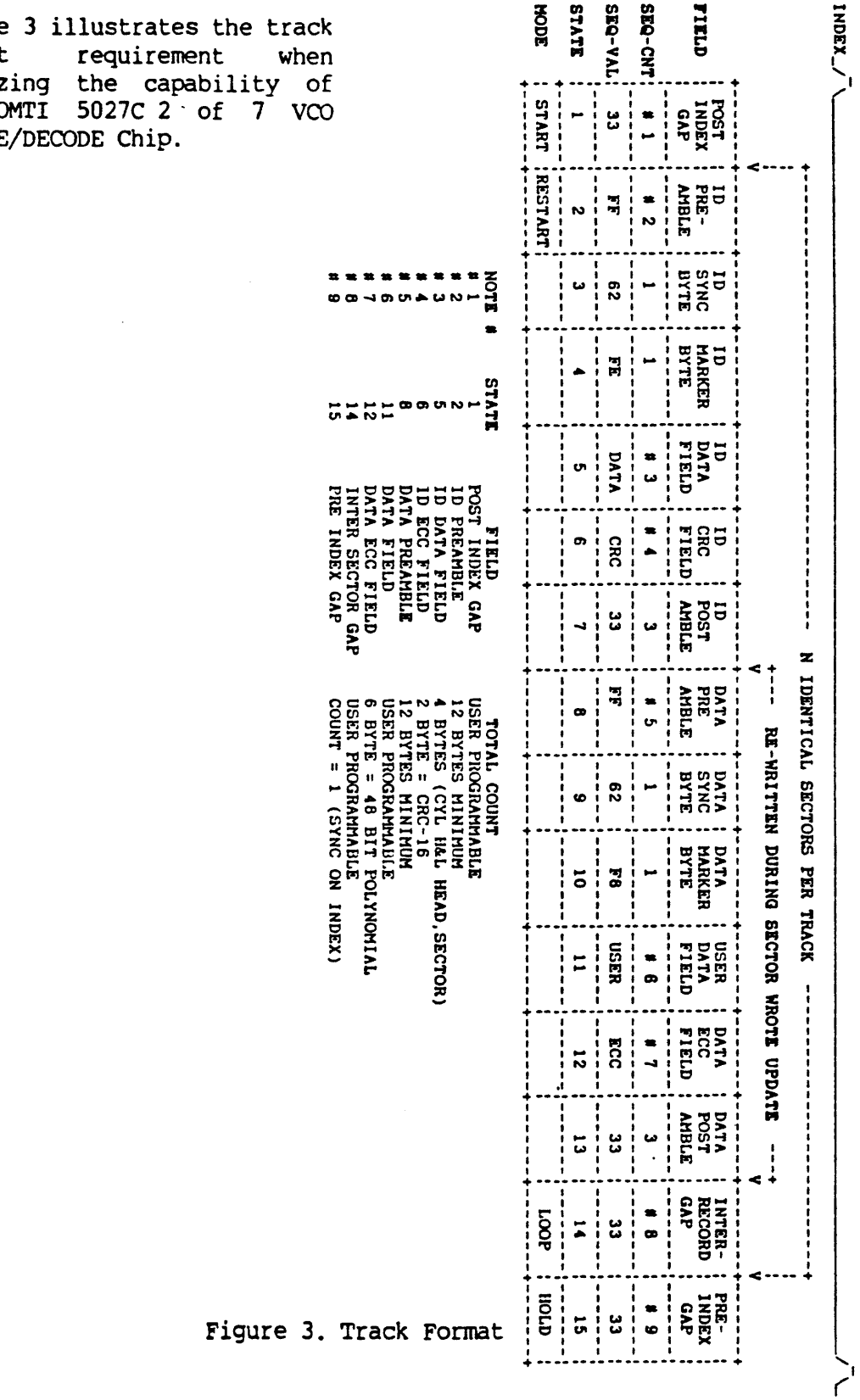
Symbol	Parameter	Min	Max	Unit
T1	NRZ_IN to RD_REF_CLK / SETUP			ns.
T2	NRZ_IN to RD_REF_CLK / HOLD			ns.
T3	AM_ENABLE to NRZ_IN / SETUP			ns.
T4	RD_REF_CLK \ TO NRZ_OUT VALID			ns.
T5	RD_REF_CLK \ TO AM_FOUND VALID			ns.

SECTION 6

DISK FORMAT

6.1 Track Format

Figure 3 illustrates the track format requirement when utilizing the capability of the OMTI 5027C 2 of 7 VCO ENCODE/DECODE Chip.



NOTE #	STATE	FIELD	TOTAL COUNT
# 1	1	POST INDEX GAP	USER PROGRAMMABLE
# 2	2	ID PREAMBLE	12 BYTES MINIMUM
# 3	5	ID DATA FIELD	4 BYTES (CYL H&L HEAD,SECTOR)
# 4	6	ID ECC FIELD	2 BYTE = CRC-16
# 5	8	DATA PREAMBLE	12 BYTES MINIMUM
# 6	11	DATA FIELD	USER PROGRAMMABLE
# 7	12	DATA ECC FIELD	6 BYTE = 48 BIT POLYNOMIAL
# 8	14	INTER SECTOR GAP	USER PROGRAMMABLE
# 9	15	PRE INDEX GAP	COUNT = 1 (SYNC ON INDEX)

Figure 3. Track Format